A LOW COST 77 GHz MONOLITHIC TRANSMITTER FOR AUTOMOTIVE COLLISION AVOIDANCE SYSTEMS

Lamberto Raffaelli, Earle Stewart, Robert Quimby,
John Borelli, Art Geissberger, Dan Palmieri
Alpha Industries
Woburn, Massachusetts

ABSTRACT

The design, integration and test results of a 77 GHz GaAs monolithic transmitter specifically optimized for low cost, large volume automotive collision avoidance systems is presented. Greater than +15 dBm of output power has been achieved at the output waveguide interface across a 1 GHz bandwidth using monolithic chips exclusively. This module, due to its small size, light weight and low production cost, is a significant advance in MMW technology from traditional waveguide hybrid approaches and it now makes collision avoidance radars affordable.

INTRODUCTION

In Europe, the 76 to 77 GHz band has already been allocated for automotive collision avoidance radars[1]. The technology required for this high volume application needs to simultaneously satisfy low cost and high reliability requirements. The processes required to produce traditional frequency sources at these frequencies (Gunn oscillators) are labor intensive and do not lend themselves to low production costs. Due to these requirements, MMIC technology finds a unique opportunity to be inserted into large volume production programs in the near future. This article presents the design and performance of a low cost 77 GHz monolithic transmitter specifically developed for the collision avoidance radar application with projected production costs fully compliant with the automotive industry requirements.

TRANSMITTER CONFIGURATION

Two monolithic technologies, both currently employed by Alpha, were considered for the automotive collision avoidance application: 1) a fundamental approach at 77 GHz using MMICs which incorporate 0.15 micron Pseudomorphic High Electron Mobility Transistors (P–HEMTs), and 2) a multiplied approach using MMICs which incorporate 0.25 micron Power Metal Semiconductor Field Effect Transistors (MESFETs) at 38.5 GHz, followed by a varactor–based MMIC doubler. Upon initial analysis, the 0.15 micron P–HEMT MMICs seemed to offer better performance and would be more appropriate for use. However, this technology is far from maturity compared to MESFET technology and has never been demonstrated in production. Therefore, the multiplied approach was selected for use in the near and mid–term. P–HEMT technology can be substituted when it is considered to be sufficiently mature for production.

The block diagram of the transmitter is shown in figure 1. This particular arrangement satisfies the needs of most collision avoidance systems and can be used to directly replace conventional VCOs. Referring to the block diagram, a MMIC MESFET VCO and two MMIC MESFET amplifiers, described in the next sections, are cascaded, providing approximately +23 dBm of output power. This power level is sufficient to efficiently drive the MMIC varactor multiplier. This guarantees a minimum of +12 dBm of power at the output of the module over a temperature range of –40°C to +70°C. The amplifiers, in addition to providing the necessary gain and power output, provide in excess of 50 dB of isolation, thereby virtually eliminating pulling effects on the VCO and the need for an isolator. A WR–10 waveguide output is provided through the use of a finline transition. The transmitter module also contains bias regulation and protection circuitry, as well as a temperature compensation circuit to minimize the frequency drift of the VCO.

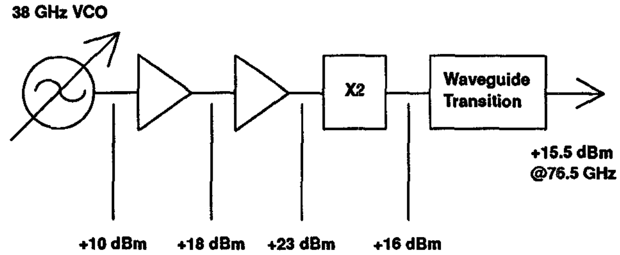

Figure 1. 38 GHz Transmitter Module Block Diagram

93CH3316-7/93/0000-0063$01.00 © 1993 IEEE

GAAS MONOLITHIC CHIPS

The monolithic chips are fabricated on 100 micron (thickness at process completion) GaAs MBE material and are based on 0.25 micron electron beam written gate technology. A track system and a 1:1 projection stepper photolithographic system are also used in wafer manufacturing for low breakage, high throughput, high repeatability and improved yields. The chips are 100% automatically tested on wafer to monitor DC and RF parameters, rejecting non–compliant components and therefore reducing module assembly cost. To further reduce costs, the chips were designed to minimize size and therefore maximize the number of chips per GaAs wafer.

VCO Chip

The 38 GHz MMIC VCO (figure 2) was originally developed for use in smart munitions and has since been used for commercial radio applications[2] in addition to automotive collision avoidance applications. The VCO uses a 0.25 x 400 micron power MESFET in common source configuration and two double mesa integrated varactors, one for frequency tuning and one for temperature compensation. Nominal tuning bandwidth is 750 MHz; however, where internal temperature compensation is not needed, the two varactors can be used in tandem to obtain a total tuning range in excess of 1.5 GHz. The double mesa varactor technology[3] was specifically designed to reduce the diode series resistance and improve the Q of the resonator, resulting in lower phase noise (–100 dBc/Hz at 1 MHz offset) as compared to a planar varactor process. The VCO chip layout has recently been optimized for production, resulting in a chip size of about 2.0 x 1.5 mm^2.

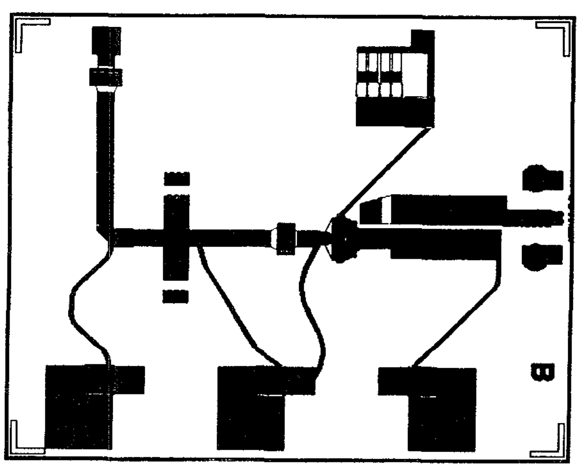

Figure 2. 38 GHz MMIC VCO

Amplifier Chips

In order to increase output power and to buffer the VCO chip, a driver amplifier (figure 3) and a power amplifier (figure 4) were developed. The amplifier chips are based on Alpha's standard 0.25 x 400 micron power MESFET process. Both amplifiers use a two–stage single–ended configuration. The amplifier designs were based on a minor modification of a technique used by Cripps[4] at lower frequencies for predicting the saturated conductance of the FET. The results of this prediction were also verified through on–wafer load–pull measurements from 34 to 40 GHz. By combining two and four 400 micron devices in the output, better than +20 and +25 dBm of saturated power was achieved in the driver and power chips, respectively. However, in order to increase production yields and reduce costs, the chip specifications were written to require only +18 dBm and +23 dBm of saturated power from the driver and power amplifiers, respectively. Small chip size was aggressively pursued in the design stage, since amplifiers were traditionally large and therefore would have the biggest impact on module cost. This aggressiveness resulted in a total area for the two chips of just over 9 mm^2 and assured a low module cost.

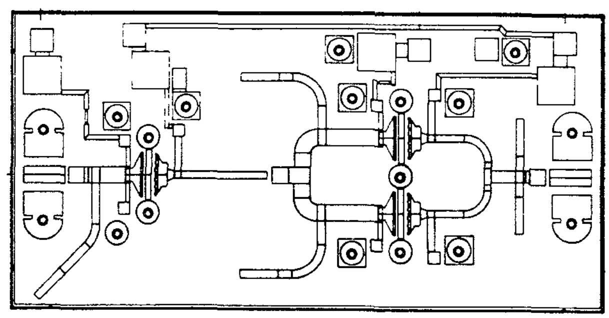

Figure 3. 38 GHz MMIC Driver Amplifier

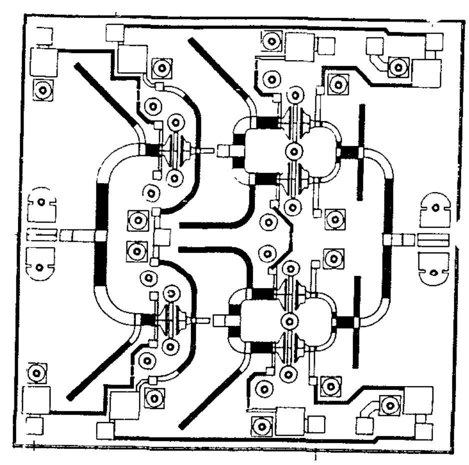

Figure 4. 38 GHz Power Amplifier

Multiplier Chip

The multiplier chip (figure 5) uses the same high Q double mesa varactor technology as the VCO chip. A well–characterized, readily available varactor diode structure (not necessarily the optimum one for this application) was selected for the circuit design. The DC parameters of the device presented an R_s of 1Ω, a zero–bias junction capacitance (C_{j0}) of 330 fF and a reverse–breakdown voltage of 12V. The device capacitance versus reverse–voltage curve exhibited the traditional non–linear characteristic and became asymptotic at higher reverse–voltage values. Computations made to determine whether this particular device was acceptable as a multiplying element revealed a dynamic cutoff–frequency of 1.82 THz and diode efficiency of 70.5%, accounting for input drive level and an abrupt–junction device type.

The design approach used was a non–linear method established by Manley & Rowe. Briefly stated, by knowing the diode characteristics, one can maximize conversion efficiency by calculating the equivalent varactor impedances as seen by the input and output signals for a given input drive level. With this knowledge, one need only transform the input characteristic impedance to the equivalent input varactor impedance while providing the output transformation in the same manner. A simple but effective matching structure has resulted in a conversion loss of less than 6.5 dB at +25°C, a large improvement over traditional planar varactor circuits at these frequencies. To optimize performance, the anode of the varactor is at DC ground while the DC operating point can be varied by applying a positive voltage to the diode cathode. To prevent the input and output signals from appearing at the undesired port, the input signal is terminated with a short circuit at the output port while the output signal is terminated with a short circuit at the input port. Both short circuits were realized using quarter–wave open circuit stubs. These terminations resulted in fundamental and third harmonic suppressions in excess of 30 dB. Circuit size has been minimized to 1.25 x 1.5 mm.

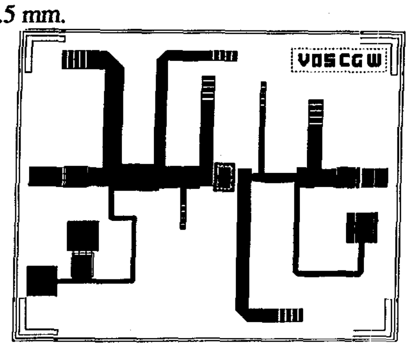

Figure 5. 38.5/77 GHz MMIC Doubler

MECHANICAL DESIGN

The production housing is a light weight, low cost aluminum package which is laser sealed for hermeticity. A metallized dielectric window and soldered feedthroughs retain hermeticity while providing all necessary input and output signals. The GaAs MMIC chips were directly attached to a gold plated housing (figure 6) with AuSn eutetic solder to reduce thermal resistance. Interconnections are made with thermal compression bonding of gold wire or ribbon. In order to reduce waveguide moding problems, the width of the cavity containing the chips was kept to a minimum by placing the all bias circuitry in a second cavity underneath the transmitter housing. DC bias for the chips is accessed by means of hermetic feedthroughs between the two cavities. The output of the multiplier chip is transitioned from microstrip to WR–10 waveguide through a low loss finline transition. Overall package size is 1.15" x 1.05" x 0.90".

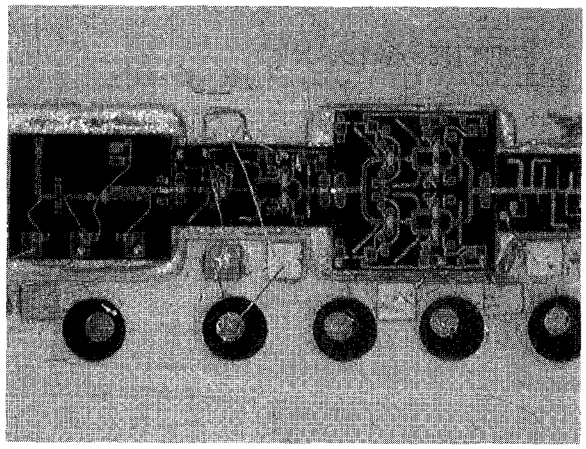

Figure 6. 77 GHz MMIC Transmitter

TEST RESULTS

Figure 7 shows typical tuning response of the 77 GHz transmitter module at –40°C, +25°C and +70°C. 1.5 GHz of tuning bandwidth was obtained over a tuning range of 2 to 12 volts. Frequency drift vs. temperature is kept to a minimum using an off chip temperature compensation circuit with the secondary varactor of the VCO chip. Average drift from –40°C to +70°C is 1 MHz/°C. Output power vs. temperature is shown in figure 8 and indicates a 1 dB bandwidth of 1 GHz. Output return loss was measured to be greater than 12 dB. Typical phase noise is –90 dBc/Hz at 1 MHz offset, as measured with a spectrum analyzer. DC bias requirements for the chips were 500 mA @ 5 volts for the amplifiers and 80 mA @ 4 volts for the VCO for a total power consumption of 2.8 watts.

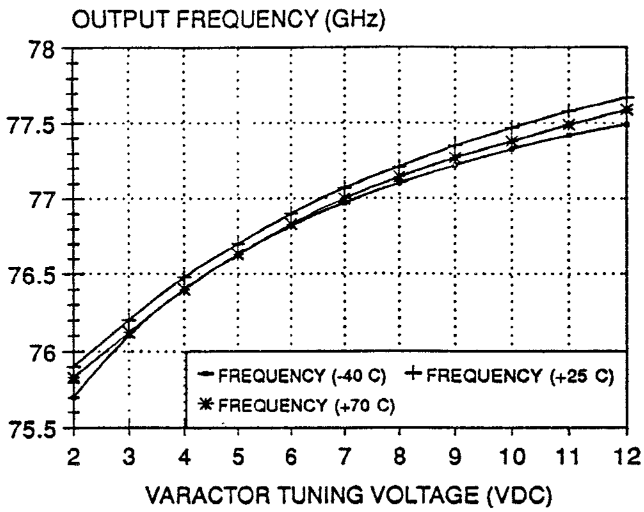

Figure 7. 77 GHz MMIC Transmitter Output Frequency vs. Tuning Voltage

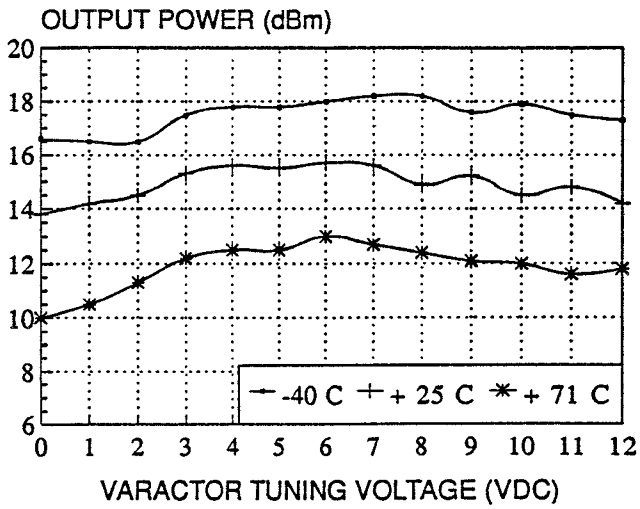

Figure 8. Transmitter Output Power

CONCLUSIONS

The 77 GHz transmitter has shown that MMW MMIC technology is ready for high volume commercial applications. The transmitter design is flexible enough to meet the technical requirements of most collision avoidance system designers. MMIC costs are now competitive with the lowest priced hybrid alternatives, and will shortly have a clear cost advantage. The biggest cost advantage is in the area of module assembly, due to reduced complexity and parts count, and in testing, since the MMICs require no tweaking or tuning. The cost of the transmitter as described in this paper is projected to be approximately $400 in quantities of 1000. Assuming production quantities of 100,000 per year, 4" wafer manufacturing and high volume assembly and testing, this cost will be around $60.

ACKNOWLEDGEMENTS

The authors would like to thank Diane Gallo and Paul Marcoaldi for the assembly and testing of the transmitter, respectively.

REFERENCES

1. Rolland, P.A., Haese, N., and Benlamih, M., "Quasi-Optical Technology for MM Wave Car Electronics", *Workshop Proceedings, European Microwave Conference*, Stuttgart, Germany, 1991.

2. Raffaelli, L., and Stewart, E., "A Standard Monolithic Tranmitter for 38 GHz PCN Applications", *Microwave Journal*, October 1992.

3. McDermott, M., Sweeney, C., Benedek, M., Borelli, J., Dawe, G., Raffaelli, L., "Integration of High-Q GaAs Varactor Diodes and 0.25 micron GaAs MESFETs for Multifunction Millimeter-Wave Monolithic Circuit Applications", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 38, No. 9, September 1990.

4. Cripps, Steve, "Old Fashioned Remedies for GaAsFET Power Amplifier Designers", IEEE MTT-S Newsletter, Summer 1991.